IN THE CLAIMS

1. (currently amended): A non-optical electronic semiconductor device comprising:

a support substrate including at least one groove;

a first [[an]] insulation layer on top of the support substrate;

an SOI layer formed on top of the first insulation layer; and

a first ~~at least one~~ element layer formed on the SOI layer; [[and]]

wherein the at least one groove ~~formed in the support substrate, the at least one groove being located~~ extends below a target element in the first element layer whose dielectric loss is to be controlled among the at least one element;

a second insulation layer formed on top of the first element layer; and

at least one additional element layer formed on top of the second insulation layer.

2. (currently amended): The semiconductor device according to claim 1, wherein the at least one groove is formed such that a reverse face of the first insulation layer is exposed.

3. (original): The semiconductor device according to claim 1, wherein the at least one element is an analog element.

4. (original): The semiconductor device according to claim 3, wherein the analog element is an inductor.

5. (original): The semiconductor device according to claim 1, wherein the support substrate is one of a silicon substrate and a sapphire substrate.

6. (currently amended): A non-optical electronic semiconductor device comprising:

a support substrate including at least one groove;

a first [[an]] insulation layer formed on the support substrate;

an SOI layer formed on the first insulation layer; and

a plurality of analog elements formed on the SOI layer;

wherein the at least one groove ~~formed in the support substrate such that the at least one groove is located~~ extends below one or more analog elements among the plurality of elements;

a second insulation layer formed over the plurality of analog elements; and

at least one additional element layer formed on top of the second insulation layer.

~~wherein the analog element is an element for which control of the dielectric loss is sought, among the plurality of analog elements.~~

7. (currently amended): The semiconductor device according to claim 6, wherein the groove is formed such that a reverse face of the first insulation layer is exposed.

8. (previously amended): The semiconductor device according to claim 6, wherein the one or more analog elements are inductors.

9. (original): The semiconductor device according to claim 6, wherein the target element is an element for which control of the dielectric loss is sought, among the plurality of analog elements.

10. (original): The semiconductor device according to claim 6, wherein the support substrate is one of a silicon substrate and a sapphire substrate.

11. (new): A non-optical electronic semiconductor device comprising:

a support substrate having a groove;

a first insulation layer formed on the support substrate;

an SOI layer formed on the first insulation layer;

a high-frequency circuit formed on the SOI layer, wherein the groove formed in the support substrate extends under the high-frequency circuit;

a second insulation layer formed over the high-frequency circuit; and

at least one additional element layer formed on top of the second insulation layer.

12. (new): The semiconductor device according to claim 11, wherein the groove is formed such that a reverse face of the first insulation layer is exposed.

13. (new): The semiconductor device according to claim 11, wherein the support substrate is a silicon substrate or a sapphire substrate.

14. (new): A non-optical electronic semiconductor device comprising:

a support substrate including a groove;

a first insulation layer formed on the support substrate;

an SOI layer formed on the first insulation layer; and

an inductor formed on the SOI layer, wherein the groove formed in the support substrate extends under the inductor;

a second insulation layer formed over the inductor; and

at least one additional element layer formed on top of the second insulation layer.

15. (new): The semiconductor device according to claim 14, wherein the groove is formed such that a reverse face of the first insulation layer is exposed.

16. (new): The semiconductor device according to claim 14, wherein the support substrate is a silicon substrate or a sapphire substrate.

17. (new): The semiconductor device according to claim 1, further comprising a plurality of bonding pads formed over the support substrate, wherein the at least one groove is absent below the plurality of bonding pads.

18. (new): The semiconductor device according to claim 6, further comprising a plurality of bonding pads formed over the support substrate, wherein the at least one groove is absent below the plurality of bonding pads.

19. (new): The semiconductor device according to claim 11, further comprising a plurality of bonding pads formed over the support substrate, wherein the groove is absent below the plurality of bonding pads.

20. (new): The semiconductor device according to claim 14, further comprising a plurality of bonding pads formed over the support substrate, wherein the groove is absent below the plurality of bonding pads.